1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There are four other appeals known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. The related appeals that are currently pending before the Board concern U.S. Patent Application Serial Numbers 08/984,560; 08/984,562; and 08/984,701. The fourth appeal was filed in U.S. Patent Application Serial Numbers 08/984,561. U.S. Patent Application Serial Numbers 08/984,561 was allowed by the examiner after the appeal brief was filed.

3. STATUS OF THE CLAIMS

Claims 36-39, 59-69, and 75-83 are currently pending and appealed. No claims have been canceled or added. The pending claims are listed in Appendix I.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action mailed January 14, 2003.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, the embodiments disclosed relate to a memory device that selectably operates using both burst and pipelined modes of operation. In one embodiment, an asynchronously addressable storage device 100 (shown in FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the

burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Pg. 29, lines 5-25). Some embodiments can switch between burst access and ... pipelined modes of operation without ceasing ("on the fly"). (Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is first used to select data within the device 100. A counter 149 included in the circuitry 122 then increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses external addresses 115 to access data within the device 100. (Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Pg. 8, lines 1-5). In addition to the embodiments described herein, other embodiments of varying scope, such as systems, methods, and storage devices, such as memory circuits, are included. (Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

1) Whether claims 36-39, 59-64, 69, and 75-83 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning, hereinafter "Manning".

2) Whether claims 65-68 were properly rejected under 35 USC § 103(a) as being unpatentable over Manning in view of U.S. Patent No. 5,587,964, issued to Rosich et al., hereinafter "Rosich".

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Establishing anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> To establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

While it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be